REMARKS

The foregoing amendment and the following remarks are responsive to the First Office Action mailed May 19, 2004 for the request of continuing examination (RCE) of parent application 09/544,762 filed April 07, 2000. Final rejection has been made to Claims 1-16 in this First Office Action. The Applicant respectfully requests that the Examiner withdraw the final rejection. The Applicant has amended Claims 1 and 8 as above. Thus, entry of the amendment is respectfully requested, and it is respectfully submitted that, as amended, all the pending claims are allowable.

Request to Withdraw Final Rejection

On the Office Action Summary, the Examiner checked "2a) this action is FINAL". It is unclear whether this action was intended or inadvertent because the Examiner did not include the form paragraphs as required by the MPEP. When making a first action final rejection, MPEP 706.07(b) requires that the Examiner use Form Paragraphs 7.41 or 7.41.03. However, the Examiner did not include those form paragraphs. As such, Applicant is unsure of the Examiner's intent. In any case, Applicant respectfully requests Examiner to withdraw final rejection and allow the amendment.

Even assuming that the Examiner intended to make first action final rejection, Applicant submits that such action is not merited in the present case. According to MPEP 706.07(b), "*it would not be proper to make final a first Office Action in a continuing or substitute application where that application contains material which was presented in the earlier application after final rejection or closing of prosecution but was denied entry because (A) new issues were raised that required further consideration and/or search, or (B) the issue of new matter was raised.*" The current application is a request of continuation of examination (RCE). This RCE contains material

that was presented in the earlier application 09/544,762 after final rejection but was denied because new issues were raised that required further consideration and/or search. Thus, it would be improper to make a first action final rejection in the present application where the amendments should be considered. Therefore, the Applicant respectfully requests the final rejection to be withdrawn.

SUMMARY

Rejection Under 35 U.S.C. 112, first paragraph

Claims 1-6 were rejected under 35 U.S.C. 112, second paragraph based on lack of antecedent basis for the limitations "said receiver photodiodes" in line 13 and "said circuit" in line 17. The limitations "said receiver photodiodes" with "said receiver photodiode" in line 13 and "said circuits" in line 17 in Claim 1 have been amended as "said receiver photodiode" and "said circuit cards", respectively. Therefore, the rejection over Claims 1-6 under 35 U.S.C. 112, second paragraph, is overcome.

Rejection Under 35 U.S.C. 103(a)

Claims 1-2, 6, 8-9, 13, and 15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad et al. (U.S. patent No: 5,818,984) in view of Davidson (US patent No: 6,160,653) and in further view of William (US patent No. 3,858,154).

Claim 1

As shown below, Applicant respectfully submits that Claim 1 should not be rejected under 35 U.S.C. 103(a). First, as understood by the Applicant, Ahmad et. al teaches only the use of chips (or integrated circuits), and does not appear to teach the use of circuit cards. Next, as understood

by the Applicant, Ahmad et al. does not appear to teach an upright relationship between chips or circuit cards. Additionally, as understood by the Applicant, Ahmad et al. appears to teaches away a plurality of circuit cards each being mounted to **one** of the circuit card connectors. As such, it appears that there is no suggestion or motivation for modifying "each chip being mounted to multiple connectors" disclosed in Ahmad et al. into "each circuit card being mounted to one connector" as claimed. Finally, as understood by the Applicant, it appears that neither Ahmad et. al, William, nor Davidson teach a shock-resistant system Therefore, Claim 1 is believed to be allowable.

Ahmad et. al Appears to Teach Only the Use of Chips (or Integrated Circuits)

As understood by the Applicant, it appears that all that Ahmad et al. teaches are chips (or integrated circuits) mounted on a substrate and interconnection between the chips. Ahmad et al. does not appear to disclose interconnection between interface cards. Further, Ahmad et al. does not appear to teach the use of circuit card connectors.

The disclosure of interconnection between integrated circuits or chips does not explicitly or implicitly teach the interconnection between the circuit cards. It is well known in the art that a chip is "[a] minute slice of a semiconducting material, such as silicon or germanium, doped and otherwise processed to have specified electrical characteristics, especially before it is developed into an electronic component or integrated circuit," *see* www.Dictionary.com; an integrated circuit is "[a] complex set of electronic components and their interconnections that are etched or imprinted on a chip," *see* id.; however, a circuit card is an electronic assembly of chips onto a single card, i.e., "a printed circuit that can be inserted into expansion slots in a computer to increase

the computer's capabilities," *see* id. Thus, although Ahmad et al. teaches interconnection between the integrated circuits, Ahmad et al. apparently fails to teach or suggest interconnection between circuit cards.

Ahmad et al. Does not Appear to Teach an Upright Relationship Between Circuit Cards

Claim 1 includes a plurality of **circuit cards connectors** for "supporting circuit cards in a generally **upright** parallel relationship." The Examiner stated that Ahmad et al. teaches "*a plurality of circuit card connectors (col. 3, lines 53-59 and 15, fig. 2) disposed in spaced apart relation thereon for supporting circuit cards in a generally upright parallel relationship (chips 14a-i are arranged in a parallel relationship with respect to each other)*". Ahmad et al. only appears to show the **parallel** relationship of the chips 14a-i with respect to each other, but apparently fails to teach the chips 14a-i being in **upright** relationship.

Ahmad et al. Appears to Teach Away a Plurality of Circuit Cards Each Being Mounted to **One** of the Circuit Card Connectors

As discussed above, the Examiner stated that Ahmad et al. teaches "*a **plurality** of circuit card connectors (col. 3, lines 53-59 and 15, fig. 2)*". In col. 3, lines 55-58, Ahmad et al. teaches:

> *Referring to FIGS. 1-3A, multi-chip module 10 comprises interconnection substrate 12 and an array of chips 14a-i arranged edge-to-edge. Chips 14a-i are connected to the substrate 12 **through pins 15. Pins 15** may be formed with controlled-collapse chip-connections (also known in the art as C4, conductive adhesive bumps or other pinless connectors generally referred to as surface mount technology.*

The teaching in col. 3, lines 55-58 cited by the Examiner does not show whether each circuit card is mounted to **one** of the connectors (pins 15) or not. However, in the only embodiment as shown in Fig. 2, Ahmad et al. appears to specifically show that each circuit card is mounted to

a **plurality** of connectors (pins 15). As understood by the Applicant, it is also well known in the art that a single pin can hardly achieve the connection between the chip and the substrate. *See e.g.* http://www.computercraft.com/docs/chips.html (explaining that a "caterpillar" contains a chip which is connected via many thin wires to the pins of the caterpillar). Therefore, Ahmad et al. appears to actually teach away "a plurality of circuit cards each being mounted to **one of the circuit card connectors**" as claimed in Claim 1.

Ahmad et. al Does Not Appear to Teach a Shock-Resistant System

Regarding Claim 1, the Examiner stated that "*Ahmad et al. discloses a shock-resistant system (10, fig. 1 and 32, fig 4) for interconnecting circuit cards (14g, 14h, fig. 1 and 34, fig. 4) to enable data to be transmitted and received therebetween (col. 3, lines 40-42, col. 5, lines 24-27)*".

Ahmad et al. appears to teach a multi-chip module 10 (fig. 1) and a data processing system 32 (fig. 4). However, the Applicant could find no mention of or teaching or suggestion of a "shock-resistant" system in the disclosure of Ahmad et al.

Conclusion

It appears that neither Davidson nor William teach the above features that Ahmad et al. fails to teach. In addition, regardless what has been disclosed in Davidson and William, there is no apparent suggestion or motivation for modifying "each chip being mounted to multiple connectors" disclosed in Ahmad et al. into "each circuit card being mounted to one connector" as claimed. Therefore, because it appears that a *prima facie* case of obviousness cannot be proved, it is respectfully submitted that Claim 1 be allowed.

Claim 8

Similarly to Claim 1, it appears that a *prima facie* case of obviousness cannot been shown with respect to Claim 8. Regarding Claim 8, as Applicant understands, Ahmad et al. fails to teach many elements of Claim 8.

Ahmad et al. Appears to Fail to Teach the use of Circuit Cards

As discussed above, Ahmad et al. appears to only disclose the use of a plurality of chips (integrated circuits) formed on a substrate and interconnection between the chips. As discussed above, a chip (or an integrated circuit) and a circuit card are entirely distinct electronic equipment. Thus, although Ahmad et al. teaches interconnection between the integrated circuits, Ahmad et al. does not appear to expressly teach or suggest interconnection between circuit cards.

Ahmad et al. Appears to Fail to Teach a Plurality of Circuit Card Connectors

Ahmad et al. appears to teach a plurality of pins for connecting the chips to the substrate. However, the teaching of the pins does not explicitly or implicitly disclose the circuit card connectors.

Ahmad et al. Appears to Fail to Teach Upright Relation Between Circuit Cards

Ahmad et al. appears to disclose a plurality of chips extending parallel with the substrate. None of the chips 14a-i, 34a-d and 36 supported by the substrates 12 and 32 appear to be in upright relationship.

Ahmad et al. Appears to Fail to Teach Each of the Circuit Cards Mounted to **One** of the Circuit Card Connector

As discussed above, the Examiner stated that Ahmad et al. teaches "*a **plurality** of circuit*

card connectors (col. 3, lines 53-59 and 15, fig. 2)". Fig. 2 of Ahmad et al. appears to show that each chip 14a-i is mounted to a **plurality** of pins 15. The Examiner compared the plurality of pins 15 to circuit card connectors in Claim 8. Following this comparison, Ahmad et al. excludes the possibility of mounting a chip, or even more unlikely, mounting an entire circuit card with the use of only one connector. Therefore, Ahmad et al. appears to actually teach away "a plurality of circuit cards each being mounted to **one of the circuit card connectors**" as claimed in Claim 8.

Conclusion

It appears that neither Davidson nor William teach the above features that Ahmad et al. fails to teach. In addition, regardless what has been disclosed in Davidson and William, there is no apparent suggestion or motivation for modifying "each chip being mounted to multiple connectors" disclosed in Ahmad et al. into "each circuit card being mounted to one connector" as claimed. Therefore, because it appears that a *prima facie* case of obviousness cannot be proved, it is respectfully submitted that Claim 8 be allowed.

Claim 15

Finally, Applicant respectfully submits that Claim 15 does not appear to be *prima facie* obvious. It appears that Ahmad et al. fails to teach many key elements of Claim 15.

Ahmad et al. Appears to Fail to Teach A Plurality of Circuit Card Connectors for Supporting Circuit cards **Extending Normal** to the Backplane in a Generally **Upright** Parallel Relationship

In the Office Action, the Examiner is silent about the feature "for supporting circuit cards **extending normal to the backplane** in a generally **upright** parallel relationship" as claimed in Claim 15. Ahmad et al. appears to only teach a plurality of chips 14a-i, 34a-d and 36 extending

parallel to the substrates 12 and 32 (figs. 1, 2 and 4). Ahmad et. al appears not to make mention or suggestion of chips "extending normal to the backplane in a generally upright parallel relationship," as taught by Claim 15.

Ahmad et al. Appears to Fail to Teach the use of Circuit Cards

As discussed above, Ahmad et al. appears to only disclose the use of a plurality of chips (integrated circuits) formed on a substrate and interconnection between the chips. A chip differs significantly from a circuit card. Thus, although Ahmad et al. teaches interconnection between the integrated circuits, Ahmad et al. apparently fails to teach or suggest interconnection between circuit cards.

Ahmad et al. Appears to Fail to Teach a Plurality of Circuit Card Connectors

Ahmad et al. teaches a plurality of pins for connecting the chips to the substrate. However, the teaching of the pins does not explicitly or implicitly disclose the circuit card connectors.

Ahmad et al. Appears to Fail to Teach a Shock-Resistant System

Regarding Claim 15, the Examiner contended that "*Ahmad et al. discloses a shock-resistant system (10, fig. 1 and 32, fig 4) for interconnecting circuit cards (14g, 14h, fig. 1 and 34, fig. 4) to enable data to be transmitted and received therebetween (col. 3, lines 40-42, col. 5, lines 24-27)*".

Truly, Ahmad et al. teaches a multi-chip module 10 (fig. 1) and a data processing system 32 (fig. 4). However, it does not appear that Ahmad et al. discloses or teaches a "shock-resistant" system.

Conclusion

As to the Applicant's understanding, the features that Ahmad et al. fails to teach were not disclosed or suggested in either Davidson or William. More importantly, it appears that the feature of "circuit cards extending normally to the backplane" will change the principle of operation of the primary reference Ahmad et al. because C4 technology used in Ahmad et al. to mount the chips on the substrate does not apparently allow the chips to extend normal to the substrate. Therefore, because Applicant believes that Claim 15 is *prima facie* obvious, it is respectfully submitted that Claim 15 be allowed.

Claims 1-14

Primary Reference Ahmad et al. Appears to Teach Away "Each Circuit Card Mounted to **one** Connector" as Claimed in Claims 1-14

Claims 1-14 should be allowed because the primary reference Ahmad et al. appears to teach away the invention claimed in Claims 1-14. Ahmad et al. apparently teaches **chips** or **integrated circuits** (14a-i in fig. 1 and 34a-d and 36 in fig. 4) mounted on a substrate (10 and 32, respectively). Each of the chips or integrated circuits 14a-i, 34a-d and 36 appears to be connected to the substrate through a **plurality of connectors** (pins 15, fig. 2 and col. 3, lines 53-59). Ahmad et al. thus appears to teach away "each of said circuit cards being mounted to **one** of said circuit card connectors" as claimed in Claim 1 and "mounting each of said circuit cards to corresponding **one** of said circuit card connectors" as claimed in Claim 8. Further, as discussed above, it is well-known in the art that the connection between a chip and a substrate can hardly be achieved by a single pin (connector).

Additionally, regardless of what has been disclosed in the secondary references (Davidson and William), there appears to be no suggestion or motivation to one of ordinary skill in the art to modify Ahmad et al. into the invention as claimed in Claims 1 and 8. Therefore, Ahmad et al. appears to not only fail to teach every element as claimed in Claims 1 and 8 and Claims 2-7 and 9-14 depending thereupon, respectively, but also apparently fails to show any suggestion or motivation for modifying the Ahmad et al. into the claimed invention. Therefore, Claims 1-14 appear to be patentable over Ahmad et al., Davidson and William.

Claims 15-16

Primary Reference Ahmad et al. Teaches Away "Circuit Cards Extending Normal to the Common Backplane" in Claims 15-16

Ahmad et al. appears to teach a plurality of chips 14a-i, 34a-d and 36 arranged **edge-to-edge**. Further, as understood, the connectors (pins 15) are formed with controlled-collapse chip-connection (C4) that does not generally allow the chips to extend normal to the backplane (substrate) in a generally upright relationship. Therefore, Ahmad et al. appears to fail to teach every element as claimed in Claims 8-16. In addition, as understood, there is no suggestion or motivation to modify Ahmad et al. into the invention as claimed in Claims 15-16.

CONCLUSION

The rejections under 35 U.S.C. 103(a) are thus respectfully traversed and a Notice of Allowance is thus respectfully solicited. Should the Examiner have any suggestions for expediting allowance of the application, please contact applicant's representative at the telephone number listed below.

Respectfully submitted,

Date: Sep 20, 2004 By: 

Bruce B. Brunda
Registration No. 28,947
STETINA BRUNDA GARRED & BRUCKER
75 Enterprise, Suite 250
Aliso Viejo, CA 92656
(949) 855-1246

C:\JESSIE\OFFICEACTION\NORTH\390Q2.DOC